WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit provided with an address conversion memory circuit for converting a logical address into a physical address, comprising:

a switching circuit which switches to the active or non-active state a circuit portion including at least a tag memory for storing a logical page address as the upper bits of the logical address and a data memory for storing a physical page address as the upper bits of the physical address of said address conversion memory circuit,

wherein said circuit portion is set to non-active state with said switching circuit during the period in which the circuit for memory access is in the active state and the circuit portion of said address conversion memory circuit is not used.

2. A semiconductor integrated circuit according to claim 1, comprising:

a setting register which sets an access mode to a main memory to any one of the virtual memory access mode for making access to a virtual memory area with the address conversion of said address conversion memory circuit and the physical memory access mode for making no access to the virtual memory area,

wherein said switching circuit sets said circuit portion to non-active state based on a state that said

access mode is set to said physical memory access mode.

3. A semiconductor integrated circuit according to claim 2, comprising:

a cache memory which stores data between a processor and the main memory,

wherein said switching circuit sets said circuit portion to non-active state while the data transfer is performed between said cache memory and main memory because miss-hit is judged in said cache memory by the memory access of said processor.

4. A semiconductor integrated circuit according to claim 1, comprising:

a register for holding the logical page address previously inputted to said address conversion memory circuit;

a first comparator for comparing a logical page address of the logical address outputted from the memory access circuit with a value of said register; and

a second comparator for comparing and judging whether the intra-page address as the remaining lower bits of the relevant logical address is included or not within a boundary area of the address range indicated by the logical page address,

wherein said switching circuit sets said circuit portion to non-active state when the logical page

address is proved to be identical to the preceding logical address based on the result of comparison by said first and second comparators and the intra-page address is not included within said boundary area.

5. A semiconductor integrated circuit according to claim 2, comprising:

a register for holding the logical page address previously inputted to said address conversion memory circuit;

a first comparator for comparing a logical page address of the logical address outputted from the memory access circuit with a value of said register; and

a second comparator for comparing and judging whether the intra-page address as the remaining lower bits of the relevant logical address is included or not within the boundary area of the address range indicated by the logical page address,

wherein said switching circuit sets said circuit portion to non-active state when the logical page address is proved to be identical to the preceding logical address based on the result of comparison by said first and second comparators and the intra-page address is not included within said boundary area.

6. A semiconductor integrated circuit according to claim 3, comprising:

a register for holding the logical page address previously inputted to said address conversion memory circuit;

a first comparator for comparing a logical page address of the logical address outputted from the memory access circuit with a value of said register;

and a second comparator for comparing and judging whether the intra-page address as the remaining lower bits of the relevant logical address is included or not within the boundary area of the address range indicated by the logical page address,

wherein said switching circuit sets said circuit portion to non-active state when the logical page address is proved to be identical to the preceding logical address based on the result of comparison by said first and second comparators and the intra-page address is not included within said boundary area.

7. A semiconductor integrated circuit provided with an address conversion memory circuit for converting logical address into physical address, comprising:

a switching circuit which switches to the active or non-active state a circuit portion including at least a tag memory for storing logical page address as the upper bits of the logical address and a data memory for storing physical page address as the upper bits of the physical address of said address conversion memory

circuit,

wherein supply of clock to said address conversion memory circuit is suspended under the control of said switching circuit during the period where said circuit portion of said address conversion memory circuit is not used and the memory access is executed using the logical address outputted from the circuit of memory access.

8. A semiconductor integrated circuit, comprising a processor which includes a plurality of sets of a decode circuit to decode instruction codes and an execution circuit to execute said instruction codes, and executes the decode process and execution process of each instruction code of a compressed instruction in the group and arrangement according to instruction location information upon receiving said compressed instruction combining the group information of instruction codes executed simultaneously and the instruction location information indicating arrangement information to suggest a set of decode circuit and execution circuit used to process each instruction code among a plurality of sets thereof,

said semiconductor integrated circuit comprising:

an expanding circuit for setting to the designated arrangement the instruction codes of the same group

which are processed simultaneously according to said instruction location information;

a detecting circuit for detecting the relevant arrangement based on said instruction location information when the arrangement where a small amount of instruction codes are used and effective instruction codes are not set is generated in a group of instruction codes which are processed simultaneously; and

a control circuit for setting the execution circuit corresponding to the arrangement where the effective instruction codes are not set to the non-active state based on the detection result of said detecting circuit during the execution period of the relevant group;

wherein said process in the expanding circuit and the detection process by said detecting circuit to the group to be set with said process in the expanding circuit are performed in the same processing cycle.

9. A semiconductor integrated circuit according to claim 8,

wherein said control circuit sets, to the non-active state, the decode circuit corresponding to the arrangement where the effective instruction codes are not set during the decode period of the relevant group based on the detection result of said detecting circuit.

10. A semiconductor integrated circuit according to claim 8,

wherein said expanding circuit comprises a buffer memory having a plurality of areas to store a plurality of instruction codes corresponding respectively to a plurality of sets of said decode circuit and execution circuit so that the instruction codes of the same group may be stored to the areas of said buffer memory corresponding to the designated arrangement based on said instruction location information.

11. A semiconductor integrated circuit according to claim 9,

wherein said expanding circuit comprises a buffer memory having a plurality of areas to store a plurality of instruction codes corresponding respectively to a plurality of sets of said decode circuit and execution circuit so that the instruction codes of the same group may be stored to the areas of said buffer memory corresponding to the designated arrangement based on said instruction location information.

12. A semiconductor integrated circuit according to claim 11,

wherein said processor can process very long instruction words of longer code length.

13. A semiconductor integrated circuit according to claim 12,

wherein said compressed instruction is the instruction in which said instruction location information is added in place of eliminating the non-executable instruction codes without any effective processes inserted when the number of instruction codes to be executed simultaneously is rather small.

14. A semiconductor integrated circuit comprising a processor which is provided with a plurality of sets of the decode circuit for decoding instruction codes and the execution circuit for executing said instruction codes and performs the decode process and execution process of each instruction code depending on the instruction in which the instruction codes of the same group to be processed simultaneously are summarized to one instruction code,

said semiconductor integrated circuit comprising:

a detecting circuit which reads said instruction into the buffer memory in the processing stage before said decode process and detects whether the non-executable instruction codes without any effective process is included or not in the relevant instruction; and

a control circuit which sets the execution circuit

of the set to which said non-executable instruction code is sent to non-active state based on the result of said detecting circuit during the execution period of the instruction codes of the same group.